# Refine Search

**Search Results -**

| Terms | Documents |
|---|---|
| L6 same test | 10 |

**Database:** US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

**Search:** L7

Refine Search | Recall Text | Clear | Interrupt

## Search History

**DATE: Monday, February 27, 2006** Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L7 | L6 same test | 10 | L7 |
| L6 | L2 same (flip-flop or latch) | 174 | L6 |
| L5 | L2 same flip-flop | 82 | L5 |
| *DB=USPT,PGPB; PLUR=YES; OP=OR* | | | |
| L4 | ('5530706'\| '5663966'\| '5673273'\| '5701308'\| '5748645')![pn] | 5 | L4 |
| *DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L3 | L2 same scan | 9 | L3 |
| L2 | reset adj1 control adj1 circuit | 1009 | L2 |
| L1 | test adj1 circuit | 24843 | L1 |

END OF SEARCH HISTORY

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Generate Collection Print

L3: Entry 1 of 9 File: USPT Jun 20, 2000

DOCUMENT-IDENTIFIER: US 6079039 A
TITLE: Test circuit and test method for testing semiconductor chip

Detailed Description Text (12):
The internal scan flip-flop SFF3 is given the internal scan mode signal SMC and performs the internal scan operation in accordance with the second internal test clock signal SCK2. A reset control circuit 15 is connected to an input side of the internal scan flip-flop SFF3. A second clock rst and the internal scan mode signal SMC are given to the reset control circuit 22. In this event, the reset control circuit 15 supplies the second clock rst to the internal scan flip-flop SFF3 when the internal scan mode signal SMC is not supplied. Consequently, the internal scan flip-flop SFF3 stores a data input signal d at a timing of the second clock rst and supplies a data output signal q.

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